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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,412	09/28/2006	Michiel Adriaanszoon Klompenhouwer	NL 040345	8540

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EXAMINER	
BOYD, JONATHAN A	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,412	KLOMPENHOUWER ET AL.	
	Examiner	Art Unit	
	JONATHAN BOYD	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application number 10/599,412 filed September 28th 2006. Claims 1-12 are currently pending and have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano et al ("Fast response IPS-LCD using feed-backward overdrive technology" IDW 2002 The Ninth International Display Workshops) (herein "Nakano").

In regards to claims 1 and 12, Nakano teaches an overdrive circuit and overdriving method for a display panel comprising a pixel having inertness (*See; Pg 213, Col. 1, last passage to Col. 2, first passage*), the circuit comprising: a means for receiving a start value and a desired value being either an input value indicating an image to be displayed, or a clipped value to supply an overdrive value to the pixel (*See; Pg 212, Col. 1, last passage to Pg 213, Col. 1, 3rd passage and Fig. 2(b) for a overdrive voltage conversion table receiving the input data and the previous actual state to supply an overdrive output voltage*), means for substituting the input value by a reachable response within one predetermined period starting from the start value to obtain the clipped value (*See; Pg. 213, Col. 1, 3rd passage and Fig. 2(b) for a conversion table for*

providing the predictive state from the previous input state to the frame buffer), and a memory for receiving the clipped value to supply the start value being the clipped value delayed over the one predetermined period (*See; Pg. 213, Col. 1, 3rd passage and Fig. 2(b) for the frame buffer for storing the predictive state from the previous input state and supplying it to the conversion table*) , wherein the means for substituting comprises a means for indicating for the start value a corresponding minimum value being reachable from the start value within one predetermined period when a minimum drive value is applied to the pixel, and a corresponding maximum value being reachable from the start value within one predetermined period when a maximum drive value is applied to the pixel (*See; Pg. 213, Col. 1, 3rd passage to Col. 2, 2nd passage and Fig. 6 where a conversion table for providing the predictive state from the previous input state provides the saturated overdrive values for transitions toward 255 or 0)*.

In regards to claim 2, Nakano teaches wherein the predetermined period is a frame period (*See; Pg. 213, Col. 1, 3rd passage and Fig. 3 for a frame time*).

In regards to claim 3, Nakano teaches wherein the means for receiving comprises a table look up circuit for providing an overdrive value for pairs of the start value and the desired value (*See; Pg 212, Col. 1, last passage to Pg 213, Col. 1, 3rd passage and Fig. 2(b) for a overdrive voltage conversion table receiving the input data and the previous actual state to supply an overdrive output voltage*).

In regards to claim 4, Nakano teaches wherein the means for indicating comprises a table look up circuit for providing the minimum value and the maximum value for the start value (*See; Pg. 213, Col. 1, 3rd passage to Col. 2, 2nd passage and Fig. 6 where a conversion table for providing the predictive state from the previous input state provides the saturated overdrive values for transitions toward 255 or 0)*.

In regards to claim 5, Nakano teaches wherein the means for indicating comprises a function circuit for generating the minimum value and the maximum value from the start value in accordance with at least one predetermined function (*See; Pg. 212, Col. 1, 2nd passage to Pg. 213, Col. 2, 2nd passage and Fig. 6)*.

In regards to claim 6, Nakano teaches wherein the table comprises for all possible start values a corresponding minimum value and a corresponding maximum value (*See; Fig. 5 and 6*).

In regards to claim 7, Nakano teaches wherein the table comprises for a subset of all possible start values a corresponding stored minimum value and a corresponding stored maximum value, and wherein the means for substituting are arranged for interpolating the minimum value and the maximum value for a start value in-between start values stored in the table from corresponding stored minimum values and stored maximum values available in the table (*See; Pg. 212, Col. 1, 2nd passage to Pg. 213, Col. 2, 2nd passage and Fig. 6)*.

In regards to claim 8, Nakano teaches wherein the means for substituting comprises a clipping means for receiving the input value representing a brightness of the pixel in a present predetermined period, the minimum value, and the maximum value to supply the clipped value being: (i) the input value if a level of the input value is higher than the minimum value and lower than the maximum value, or (ii) the minimum value if the input value is equal to or lower than the minimum value, or (iii) the maximum value if the input value is equal to or higher than the maximum value (*See; Pg. 213, Col. 1, 3rd passage to Col. 2, 2nd passage and Fig. 6 where a conversion table for providing the predictive state from the previous input state provides the saturated overdrive values for transitions toward 255 or 0)*.

In regards to claim 10, Nakano teaches a display panel (*See; Fig. 1*).

In regards to claim 11, Nakano teaches signal processing circuitry (*See; Fig. 2b*).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al ("Fast response IPS-LCD using feed-backward overdrive technology" IDW 2002 The Ninth International Display Workshops) (herein "Nakano") in view of Halfant (2005/0184948).

In regards to claim 9, Nakano is silent to wherein the table look up circuit comprises difference overdrive values representing a difference between the desired value and the overdrive value, and in that the feedback overdrive circuit further comprises an adder for summing the difference overdrive values and the corresponding desired values.

However Halfant teaches a table look up circuit comprises difference overdrive values representing a difference between the desired value and the overdrive value (*See; p[0048] where the extended overdrive table comprises the difference between the overdrive value and the target value, referred to as the deficit*), and in that the feedback overdrive circuit further comprises an adder for summing the difference overdrive values and the corresponding desired values (See; p[0048] where the deficit is further added to the saturation voltage).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the overdrive table as taught by Nakano with Halfant's extended overdrive table to extend the unsaturated region to reduce interpolation errors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN BOYD whose telephone number is (571)270-7503. The examiner can normally be reached on Mon - Fri 6:00 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. B./
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629